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EXAMINER	
SITTA, GRANT	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,417	CHO ET AL.	
	Examiner	Art Unit	
	GRANT D. SITTA	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _23 October 2009_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-5,7,8 and 10-44_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-5,7,8 and 10-44_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _15 April 2004_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _10/23/2009_.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 7-8, 10-36, and 41-44 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al (6,943,757) hereinafter, Huang.

3. In regards to claim 1, Huang teaches a plasma display, comprising (abstract):

a panel <u>forming an equivalent panel capacitor</u> (abstract, "panel" fig. 1 and claim 1);

at least one voltage source for supplying a sustain voltage to the panel (fig. 10 89-91);

an inductor for recovering an energy stored in the panel by a resonance phenomenon such that the recovered energy is reusable for driving the panel (fig. 10 81 and figs. 8-9); and

first (fig. 10 (84)) and second switches arranged (fig. 10 (83)), in parallel (fig. 10 parallel) between the inductor and the panel (located in between ground) capacitor, <u>wherein an electrically conductive path from a first conductor of the panel capacitor to a</u>

<u>second conductor of the panel capacitor via the first switch is formed without passing through a ground (fig. 8 and fig. 9 current path), and</u>

wherein the inductor stores energy recovered from the panel when the first switch is on and the inductor applies the stored energy to the panel when the second switch is on (fig. 7 54 and col. 6, lines 15-43), and wherein the inductor stores the energy at a time when a sustain voltage supplied to the panel is clamped at a predetermined voltage (fig. 10 (83) and fig. 8 col. 5, lines 30-67).

4. In regards to claim 7, Huang teaches a plasma display comprising (abstract):

a display having a plurality of electrodes and having a corresponding capacitance between first and second nodes (fig. 8 A and B);

an inductor coupled to the second node and a third node (fig. 8 A and ground); a first switch coupled between the first and third nodes (fig. 10 (83)); and a second switch coupled between the first and third nodes (fig. 10 (84)), the first and second switches being formed in parallel (fig. 10 83 and 84 in parallel), wherein a first current path is formed via the panel capacitance, the second node, the inductor, the third node, the first switch and the first node, and a second current path is formed via the panel capacitance, the first node, the second switch, the third node, the inductor and the second node (col. 6, lines 15-43), and

wherein the second current path passes energy from the panel capacitance for storage in the inductor when the second switch is on, and the first current path applies

the stored energy from the inductor to the panel capacitance when the first switch is one (col. 6, lines 15-43) and wherein the inductor stores energy recovered from the panel capacitance and a sustain voltage applied to the panel capacitance is clamped at a predetermined voltage when the second switch is on (fig. 7 (54)).

5. In regards to claim 19, Huang teaches display panels having panel electrodes and corresponding panel capacitance between first and second nodes, an inductor coupled to the second node and a third node, a first switch coupled between the first and third nodes and a second switch coupled between the first and third nodes, the first and second switches being formed in parallel, an energy, efficient method of driving said display panels through the inductor coupled to the panel electrodes, comprising (fig. 10 (83,84) col. 5-6, lines 30-43):

(a) discharging the panel capacitance through said inductor initially while storing energy in said inductor (fig. 8 (52)) until the magnitude of the inductor current reaches a maximum through a first current path formed via the panel capacitance, the second node, the inductor, the third node, the first switch and the first node, and secondly charging the panel capacitance through said inductor while removing the stored energy from said inductor until the inductor current reaches zero or before zero via the first current path (fig. 10 83,85, 89); and

(b) discharging the panel capacitance through said inductor initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum through a second current path formed via the panel capacitance, the first node, the

second switch, the third node, the inductor and the second node, and secondly charging the panel capacitance through said inductor while removing the stored energy from said inductor until the inductor current reaches zero or before zero through the second current path (fig. 10 (84, 86, 82)),

wherein said inductor stores said energy while the panel capacitance (fig. 8 (52)) is clamped at first predetermined voltage and wherein said energy is removed from said inductor to cause the panel capacitance to change to a second predetermined voltage (fig. 7 (54)) wherein an electrically conductive path from a first conductor of the panel capacitor to a second conductor of the panel capacitor via the first switch is formed without passing through a ground (fig. 8 and fig. 9 current path).

6. In regards to claim 25, Huang teaches a plasma display panel driver circuit comprising (abstract):

a panel inter-electrode capacitor provided between at least one of a plurality of scanning electrodes and a plurality of sustain electrodes of a panel (fig. 1 scan and sustain eletrodes);

a charging/discharging circuit connected in series with said panel inter-electrode capacitor and between first and second nodes (fig. 10 (83,84, 87 and 88)),

a clamping circuit having first and second switches for clamping a terminal voltage across the panel inter-electrode capacitor to a first power source voltage level (fig. 10 (89)) and to a second power source voltage level (fig. 10 (90)), said first switch being connected in series between the first node and the first power source voltage

level (fig. 10 (85)), said second switch being connected in series between said first node and the second power source voltage level (fig. 10 (86)), said inter-electrode capacitor being connected in series to the first and second nodes and said charging/discharging circuit and said clamping circuit being coupled in parallel between the first and second nodes (fig. 10(82, 85 and 86)),

wherein said charging/discharging circuit comprises a pair of switches coupled in parallel to each other between the first node and a third node and an inductive coil coupled in series between the second and third nodes (fig. 10 83 and 84)),

wherein the inductive coil (fig. 10 (81)) stores energy recovered from the panel inter-electrode capacitor when a first one of the pair of switches is turned on and the inductive coil applies the stored energy to the panel inter-electrode capacitor when a second one of the pair of switches is turned on, and wherein the inductive coil is coupled to the first power source voltage level and the second power source voltage level along signal paths that do not pass through any of the first or second switches or the pair of switches(fig. 10 81, figs 8-9 ; and col. 3-4, lines 57-24).

7. In regards to claim 34, Huang teaches a plasma display comprising (abstract):

a panel forming an equivalent panel capacitor (abstract, “panel" fig. 1 and claim 1) and (fig. 10 (82));

at least one voltage source for supplying a sustain voltage to the panel (fig. 10 (89, 90 and 91));

an inductor for recovering an energy stored in the panel by a resonance phenomenon such that the recovered energy is reusable for driving the panel (fig. 10 81, figs 8-9 ; and col. 3-4, lines 57-24)

first and second switches arranged, in parallel, between the inductor and the panel, <u>wherein an electrically conductive path from a first conductor of the panel capacitor to a second conductor of the panel capacitor via the first switch is formed without passing through a ground (fig. 8 and fig. 9 current path),</u>

wherein the inductor stores energy recovered from the panel when the first switch is on and the inductor applies the stored energy to the panel when the second switch is on (fig. 10 83 and 84), and wherein the inductor is the only circuit element for storing energy recovered from the panel capacitor (fig. 10 (81)).

8. In regards to claim 36, a plasma display comprising (abstract):

a panel<u> forming an equivalent panel capacitor</u> (abstract, “panel" fig. 1 and claim 1) and (fig. 10 (82));

at least one voltage source for supplying a sustain voltage to the panel (fig. 10 (89, 90 and 91));

an inductor for recovering an energy stored in the panel by a resonance phenomenon such that the recovered energy is reusable for driving the panel (fig. 10 81, figs 8-9 ; and col. 3-4, lines 57-24);

first and second switches arranged, in parallel, between the inductor and the panel (fig. 10 83, 84, 87 and 88) <u>wherein an electrically conductive path from a first</u>

conductor of the panel capacitor to a second conductor of the panel capacitor via the first switch is formed without passing through a ground (fig. 8 and fig. 9 current path),

and a clamping circuit to clamp a panel capacitor to the at least one voltage source within a time period when the inductor stores energy, output from the panel capacitor, wherein a voltage of the panel capacitor is maintained at a substantially constant level while the inductor stores the energy output from the panel capacitor (fig. 10 85,86,89 and 90),

wherein the inductor stores energy recovered from the panel when the first switch is on and the inductor applies the stored energy to the panel when the second switch is on, wherein at least one voltage source comprises: a first voltage source for charging the panel to a first polarity voltage; and a second voltage source for charging the panel to a second polarity voltage different from the first polarity voltage, and wherein the first polarity voltage and the second polarity voltage have a same absolute value (fig. 7 (54) and col. 5 30-67 and col.. 6, lines 15-40).

9. In regards to claim 2, Huang teaches the plasma display as claimed in claim 1, wherein at least one voltage source comprises: a voltage source for charging the panel to a first polarity- voltage; and a second voltage source for charging the panel to a second polarity voltage different from the first polarity voltage (col. 5, lines 30-67).

10. In regards to claim 3, Huang teaches the plasma display as claimed in claim 2, further comprising: a third switch for forming a conductive path between the first voltage

source and the panel; and a fourth switch for forming a conductive path between the second voltage source and the panel (fig. 10 85 and 86).

11. In regards to claim 4, Huang teaches the plasma display as claimed in claim 1, further comprising: a first diode connected between the first switch and the panel; and a second diode connected between the second switch and the panel (fig. 10 87 and 88).

12. In regards to claim 8, Huang teaches the plasma display of claim 7, wherein the direction of the first and second current paths are opposite directions (fig. 8 and 9 I).

13. In regards to claim 10, Huang teaches the plasma display of claim 7, wherein the display capacitance is charge or discharged based on an LC resonance frequency (col. 3-4, lines 58-24 inherent with LC time constant).

14. In regards to claim 11, Huang teaches the plasma display of claim 10, wherein the display capacitance is charged or discharged based on a non-LC resonance frequency (col. 3-4, lines 58-24 inherent with LC time constant).

15. In regards to claim 12, Huang teaches the plasma display of claim 11, wherein an energy of the inductor current is increased prior to the discharging of the display capacitance or the energy is decreased prior to charging of the display capacitance (fig.

7 54 and col. 3-4, lines 58-24)

16. In regards to claim 13, Huang teaches the plasma display of claim 11, wherein during charging or discharging, the display capacitance is clamped before a stored energy of inductor reaches zero (fig. 7 62 and 56).

17. In regards to claim 14, Huang teaches the plasma display of claim 7, wherein the first current path further comprises a diode coupled between the first switch and the first node (fig. 10 87 or 88).

18. In regards to claim 15, Huang teaches the plasma display of claim 7, wherein the second current path further comprises a diode coupled between the first node and the second switch (fig. 10 87 or 88).

19. In regards to claim 16, Huang teaches Original) The plasma display of claim 7, further comprising: a first clamping circuit coupled between the first and second nodes; and a second clamping circuit coupled between the first and second nodes (fig. 10 85 and 89).

20. In regards to claim 17, Huang teaches the plasma display of claim 16, wherein the first clamping circuit comprises a third switch coupled to the first node and a first potential via a first conductive path (fig. 10 85), and the second clamping circuit

comprises a fourth switch coupled to the first node and a second potential via a second conductive path, wherein the first and second potentials are different (fig. 10 86, 90 and col . 5, lines 30-67).

21. In regards to claim 18, Huang teaches the plasma display of claim 17, wherein the first potential is provided by a positive power source, and the second potential is provided by a negative power source (col. 5, lines 30-67).

22. In regards to claim 20, Huang teaches the method of claim 19 further comprising: maintaining panel capacitance after step (a) by a first clamping circuit having a third switch coupled to the first node and a first potential via a first conductive path; and maintaining the panel capacitance after step (fig. 10 (85 and 89)) (b) by a second clamping circuit having a fourth switch coupled to the first node and a second potential via a second conductive path (fig. 10 (86 and 90)).

23. In regards to claim 21, Huang teaches the method of claim 20, wherein storing and removing of stored energy in the inductor is based on an LC resonance frequency if the inductor current reaches zero (col. 3-4, lines 58-24 inherent with LC time constant).

24. In regards to claim 22, Huang teaches the method of claim 20, wherein charging and discharging of the panel capacitance is not based on an LC resonance frequency via the first and second clamping circuit clamping the panel capacitance prior to the

inductor current reaching zero (col. 3-4, lines 58-24 with LC time constant).

25. In regards to claim 23, Huang teaches the method of claim 22, wherein the first and second clamping circuits clamp the panel capacitance prior to the inductor current reaches zero (fig. 7 (54)).

26. In regards to claim 24, Huang teaches the method of claim 22, wherein the second clamping circuit pre-stores energy in the inductor prior to step (a) and the first clamping circuit pre-stores energy in the inductor prior to step (b) (col. 5, lines 30-67).

27. In regards to claim 26, Huang teaches the plasma display panel driver circuit of claim 25, wherein each of the pair of switches comprises a first transistor and a diode, and the pair of switches provide opposite current paths (fig. 10 83, 87, 88 and 84).

28. In regards to claim 27, Huang teaches (Original) The plasma display panel driver circuit of claim 25, wherein the inter- electrode capacitor is charged/discharged based on an LC resonant frequency of the inductor coil and the inter-electrode capacitor (col. 3-4, lines 58-24).

29. In regards to claim 28, Huang teaches the plasma display panel driver circuit of claim 25, wherein the inter- electrode capacitor is charge/discharged based on a non-LC resonant frequency of the inductor coil and the inter-electrode capacitor (col. 3-4,

lines 58-24).

30. In regards to claim 29, Huang teaches the plasma display panel driver circuit of claim 28, wherein the clamping circuit clamps the inter-electrode capacitor one of the first and second power source voltage level prior to an energy of the inductor coil reaching zero (col. 5, lines 30-67).

31. In regards to claim 30, Huang teaches the plasma display panel driver circuit of claim 29, wherein the clamping circuit increases an energy of the inductor coil prior to charging/discharging of the inter-electrode capacitor (col. 5, lines 30-67).

32. In regards to claim 31, Huang teaches the plasma display panel driver circuit of claim 25, wherein each of said first and second switches comprises a transistor (col. 4, line 67).

33. In regards to claim 32, Huang teaches the plasma display as claimed in claim 1, wherein the inductor stores the energy during a time when the sustain voltage supplied to the panel is clamped at a negative voltage (fig. 7 and fig. 8 V3-V1).

34. In regards to claim 33, Huang teaches the plasma display as claimed in claim 32, wherein the second switch is turned on to allow the inductor to apply the stored energy to the panel when the sustain voltage is to rise to a positive voltage (fig. 7 54 and fig. 9

V2-V1).

35. In regards to claim 35, Huang teaches the plasma display as claimed in claim 34, wherein the inductor is to store energy recovered from the panel capacitor at a time when a sustain voltage supplied to the panel is clamped at a negative voltage, and wherein the inductor is to apply the stored energy to the panel capacitor during at a time when the sustain voltage is to rise to a positive polarity (fig. 7 (54)).

36. In regards to claim 41, Huang teaches the plasma display as claimed in claim 1, wherein the energy stored in the inductor is maintained at a substantially constant level during said time (fig. 7 (60) or (85)).

37. In regards to claim 42, Huang teaches the plasma display as claimed in claim 1, wherein a panel capacitor coupled to the inductor is maintained at a substantially constant voltage during said time (fig. 54 during 60 or 62).

38. In regards to claim 43, Huang teaches the plasma display as claimed in claim 1 wherein energy of the inductor current is increased independent from a panel capacitor (fig. 10 85).

39. In regards to claim 44, Huang teaches the plasma display as claimed in claim 1, wherein energy of the inductor is decreased independent from a panel capacitor (fig. 10 86).

Claim Rejections - 35 USC § 103

40. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

41. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

42. Claims 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang.

43. In regards to claim 37, Huang teaches a plasma display comprising (abstract):

a panel (abstract, “panel" fig. 1 and claim 1);

at least one voltage source for supplying a sustain voltage to the panel (fig. 10 (89, 90 and 91));

an inductor for recovering an energy stored in the panel by a resonance phenomenon such that the recovered energy is reusable for driving the panel (fig. 10 81, figs 8-9 ; and col. 3-4, lines 57-24);

first (fig. 10 (84) and second switches (fig. 10 (83)) arranged, in parallel, between the inductor and the panel (fig. 10 83) Examiner notes grounds are connected together and thus in-between 81 and 82)

wherein the inductor stores energy recovered from the panel when the first switch is on and the inductor applies the stored energy to the panel when the second switch is on (fig. 10 (84)),

wherein the first switch has a first terminal <u>directly connected via a conductor line</u> (fig. 10 (84) to the inductor (fig. 10 (81) and a second terminal coupled to the panel, wherein the second switch has one terminal <u>connected via a conductor line</u> to the first terminal of the first switch and another terminal coupled to the second terminal of the first switch (col. 6, lines 15-43), and wherein the inductor is the only circuit that stores energy, recovered from the panel (fig. 10 (81)).

Huang does not disclose expressly the second switch has one terminal <u>*directly*</u> connected via a conductor line to the first terminal of the first switch.

Huang discloses wherein a diode is connected in between the second switch and the first terminal, e.g. fig. 10 87 is switched locations with Applications D1. However, the components are functional equivalents for shutting off a backward current from the respective switch. According to <u>In re Japikse</u>, 86, USPQ 70 (CCPA 1950) a mere shift in location of parts is well within the ability of one of ordinary skill in the art. Examiner's

contention of obvious choice in design can be overcome if applicant establishes unexpected results.

44. In regards to claim 39, Huang teaches an energy recovery method for a plasma display, comprising (abstract):

forming a first electrically conductive path between a first voltage source and the plasma display using a first switch (fig. 10 85 and 89);

forming a second electrically conductive path between a second voltage source and the plasma display using a second switch (fig. 10 86 and 90));

forming a third electrically conductive path between the inductor and the plasma display using a third switch (fig. 10 81 and 83); and

forming a fourth electrically conductive path between the inductor and the plasma display using a fourth switch connected, in parallel, to the third switch, wherein the third switch has a first terminal coupled to the inductor and a second terminal coupled to the plasma display (fig. 10 84 and 81),

wherein the fourth switch has one terminal coupled to the first terminal of the third switch and another terminal <u>directly connected via a conductor line</u> to the second terminal of the third switch, and wherein the inductor is <u>connected via a conductor line</u> to the first voltage source and the second voltage source along signal paths that do not pass through any of the first or second switches or the pair of switches (fig. 10 81, figs 8-9 ; and col. 3-4, lines 57-24).

Huang does not disclose expressly the second switch has one terminal *directly* connected via a conductor line to the first terminal of the first switch.

Huang discloses wherein a diode is connected in between the second switch and the first terminal, e.g. fig. 10 87 is switched locations with Applications D1. However, the components are functional equivalents for shutting off a backward current from the respective switch. According to In re Japikse, 86, USPQ 70 (CCPA 1950) a mere shift in location of parts is well within the ability of one of ordinary skill in the art. Examiner's contention of obvious choice in design can be overcome if applicant establishes unexpected results.

45. In regards to claim 38, Huang teaches the plasma display as claimed in claim 37, wherein the second terminal of the first switch is coupled to the panel through a first diode, and wherein said another terminal of the second switch is coupled to the panel through a second diode (fig. 10 87 and 88).

46. In regards to claim 40, Huang teaches the energy recovery method as claimed in claim 39, wherein the second terminal of the third switch is coupled to the plasma display through a first diode, and wherein said another terminal of the fourth switch is coupled to the panel through a second diode (fig. 10 87 and 88).

47. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Iseki et al (6,483,487) hereinafter, Iseki

48. In regards to claim 5, Huang teaches an energy recovering method for a plasma display, comprising (abstract, col. 1-4):

forming a first electrically conductive path between a first voltage source and the plasma display using a first switch (fig. 10 (85));

forming a second electrically conductive path between a second voltage source and the plasma display using a second switch (fig. 10 (86));

forming a third electrically conductive path between an inductor and the plasma display using a third switch (fig. 10 (84)); and

forming a fourth electrically conductive path between the inductor and the plasma display using a fourth switch connected, in parallel, to the third switch (fig. 10 (83)), said method further comprising:

shutting off a backward current from the plasma display using a first diode connected between the third switch and the plasma display (fig. 10 (88)); and

shutting off a backward current from the fourth switch using a second diode connected between the fourth switch and the plasma display, wherein the inductor stores energy recovered from the plasma display (col. 5-6, lines 30-43) and a sustain voltage applied to the plasma display is clamped at a predetermined voltage when the second switch is closed (fig. 7 (54)).

Huang fails to teach wherein the inductor stores energy recovered from the plasma display <u>without using a ground.</u>

However, Iseki teaches wherein the inductor stores energy recovered from the plasma display without using a ground (fig. 1 1/2 Vs and -1/2 Vs and fig. 2a-2e and corresponding Ps+ and Ps- (col. 7, lines 7-41 see also col. 7-8, lines 61-40).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Huang to include the use of wherein an inductor stores energy recovered from a plasma display without using a ground as taught by Iseki in order to provide a plasma with improved write discharge and sustain discharge characteristics and driving method of the display as stated in (col. Col. 5, lines 47-67 of Iseki). Examiner notes fig. 10 of the Huang the ground connections are already connected as common nodes and is applying the teachings Iseki to shift the voltage such to produce Ps+ and Ps- for improved discharge and higher resolution.

Response to Arguments

49. Applicant's arguments with respect to claims 5, and 37-40 have been considered but are moot in view of the new ground(s) of rejection.

50. Applicant's arguments filed 10/23/2009, with respect to claims have been fully considered but they are not persuasive.

51. In regards to claim 1, Applicant contends the prior art or record fails to teach a "capacitor wherein an electrically conductive path from a first conductor of the panel capacitor to a second conductor of the panel capacitor via the first switch is formed **without passing through a ground.**" Examiner respectfully disagrees. Examiner

contends the **path** passes from a first conductor and a second conductor without passing through ground, e.g. I in illustrative figs. 8 and 9 of Huang. The current **loop** includes ground however; the path does not have to pass **through** ground.

52. In regards to claim 7. Applicant contends the prior art of record fails to teach a sustain voltage applied to the panel capacitance is clamped at a predetermined voltage when the second switch is on. Examiner respectfully disagrees. With regards to fig. 7 of Huang 56 and 58 would correspond with switches 83 and 84. Examiner is contending 56 is on, but transitioning to off, during the third period while 54 is initially clamped at V3-V1.

53. In regards to claim 25, Applicant contends Huang does not disclose an inductive coil in series between the second and the third notes." Examiner respectfully disagrees. The inductive coil is connected between the second and third nodes through ground. Examiner notes ground is a common node through which the components are connected.

Conclusion

54. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GRANT D. SITTA whose telephone number is (571)270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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